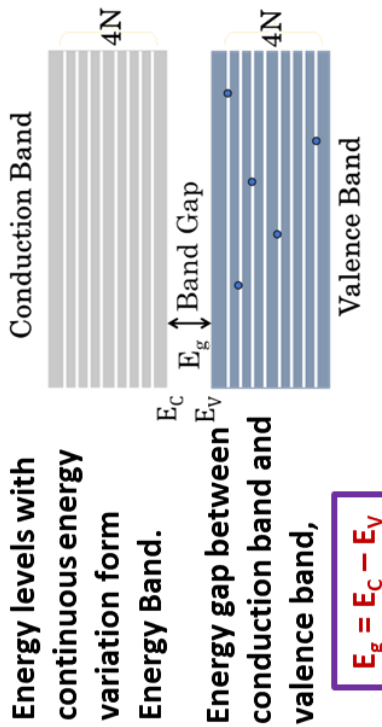
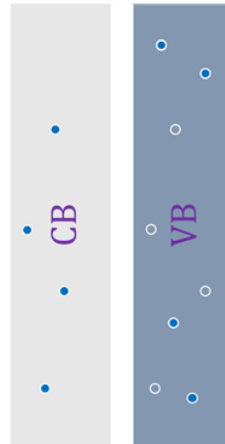


MIND MAP

Semiconductor Electronics



Intrinsic Semiconductor



In intrinsic semiconductor, the number of free electrons, n_e , is equal to the number of holes, n_h

$$n_e = n_h = n_i \text{ (Intrinsic carrier concentration)}$$

At thermal equilibrium

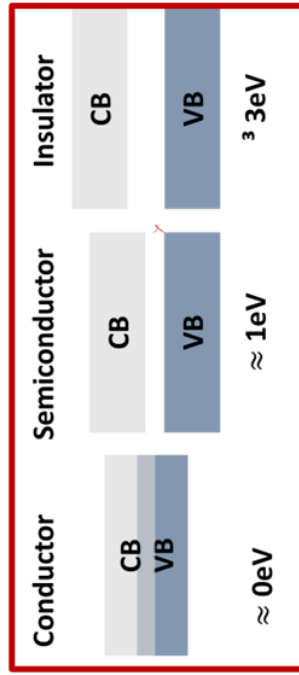
Generation rate = Recombination rate

$$n_e \times n_h = n_i^2$$

- The deliberate addition of desirable impurity is called Doping.
 - Added impurity atoms are called Dopants.
- There are two types of dopants used in doping

(a) **Pentavalent** : Arsenic (As), Antimony (Sb), Phosphorous (P)

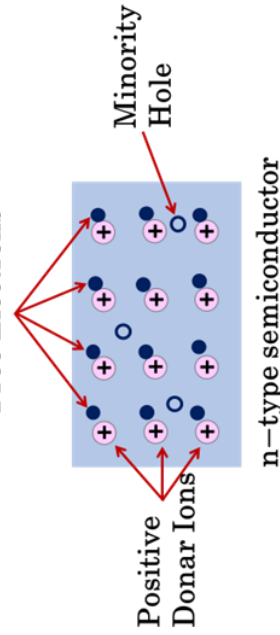
(b) **Trivalent** : Indium (In), Boron (B), Aluminium (Al)



Extrinsic Semiconductor

1. **n-type semiconductor** $n_e \gg n_h$

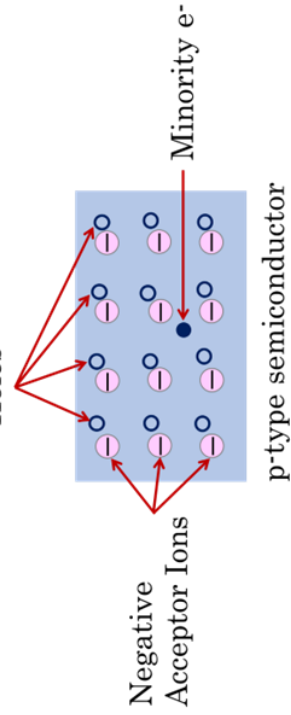
Free Electrons



n-type semiconductor

2. **p-type semiconductor** $n_h \gg n_e$

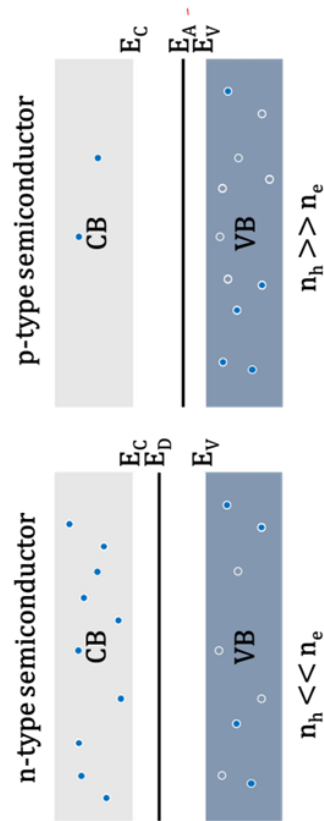
Holes



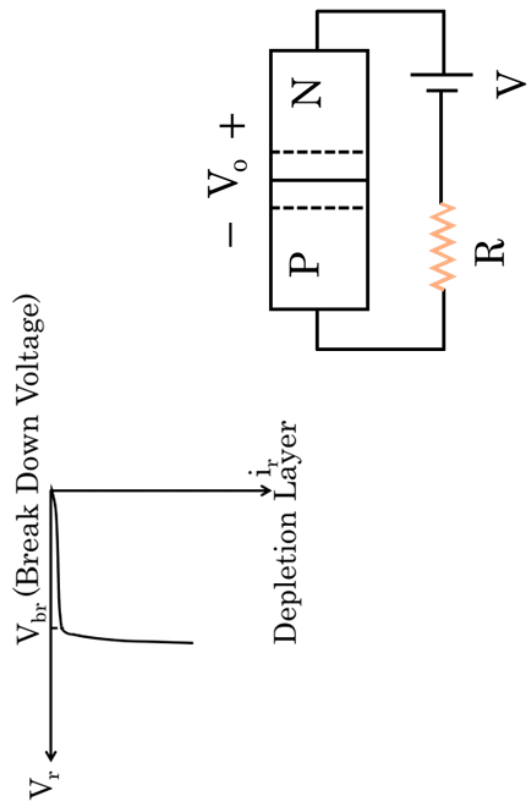
p-type semiconductor

In extrinsic semiconductor the electron and hole concentration in a semiconductor in the thermal equilibrium is given by

$$\text{Mass action law } n_e \times n_h = n_i^2$$



p-n Junction Diode Under Reverse Bias



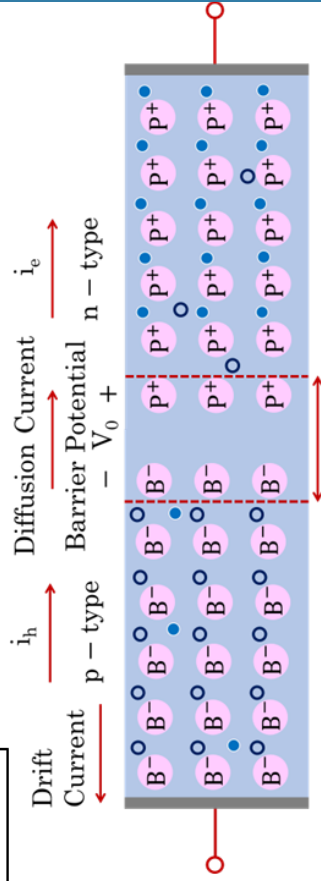
MIND MAP

Semiconductor Electronics

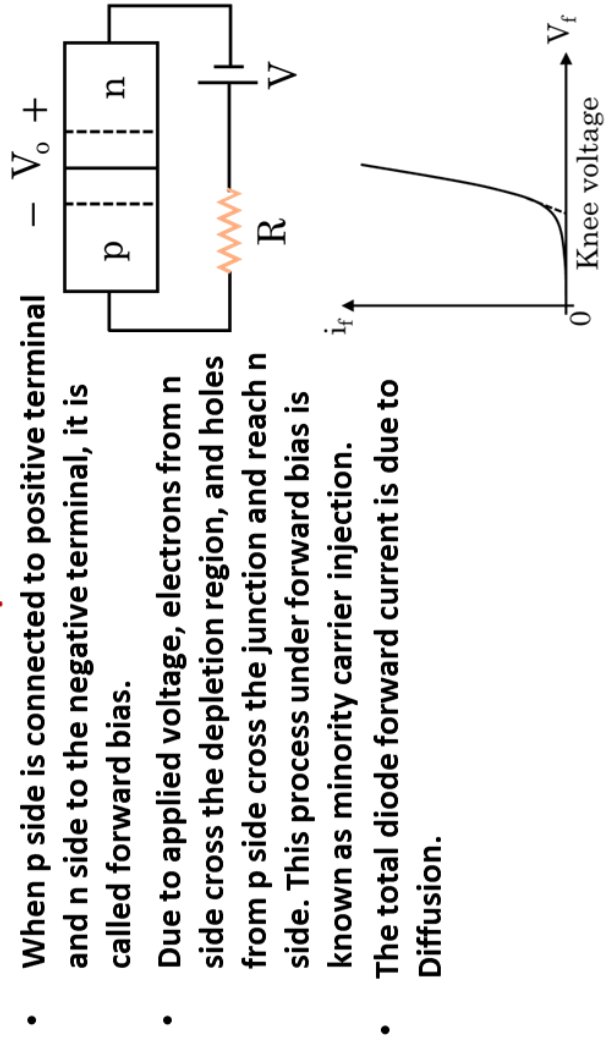
p-n Junction Diode

$$\text{Si : } V_o = 0.7 \text{ eV}$$

$$\text{Ge : } V_o = 0.3 \text{ eV}$$



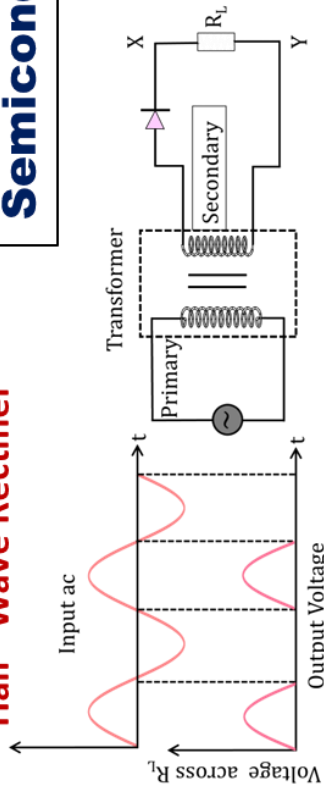
p-n Junction Under forward bias



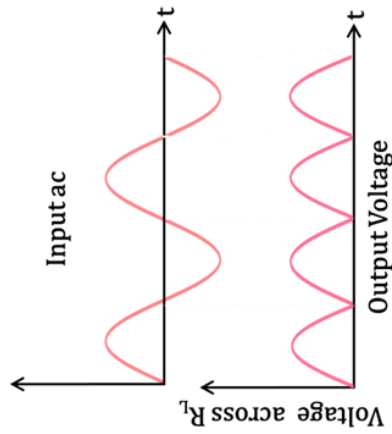
MIND MAP

Semiconductor Electronics

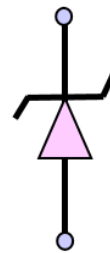
Half—Wave Rectifier



Full—Wave Rectifier



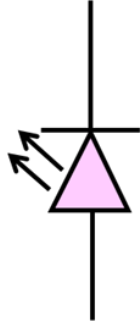
Zener Diode



Zener diode acts as a Voltage Regulator.

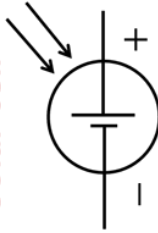
Light Emitting Diode

It is a heavily doped p-n junction which under forward bias emits spontaneous radiation.



On recombination, the energy is released in the form of photons.

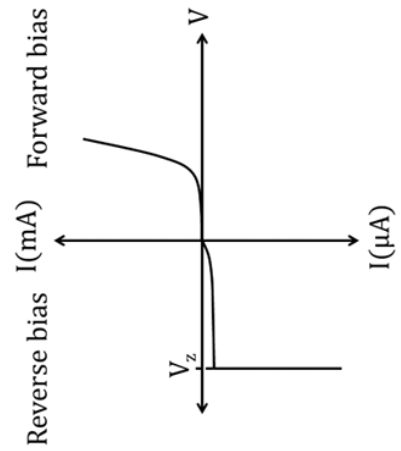
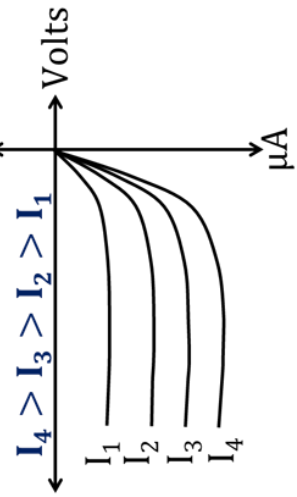
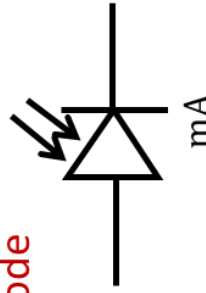
Solar cell



Electron – hole pair generated due to light with $h\nu > E_g$.

Photodiode

Photodiode operated under reverse bias.



MIND MAP

Semiconductor Electronics

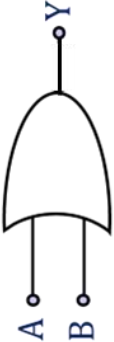
Logic Gates

NOT Gate



Input		Output
A	Y	
0	1	
1	0	

OR Gate



Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

AND Gate



Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

NAND Gate



Input		Output		
A	B	AND	NOT	NAND
0	0	0	1	1
0	1	0	1	1
1	0	0	1	1
1	1	1	0	0

NOR Gate



Input		Output		
A	B	OR	NOT	NOR
0	0	0	1	1
0	1	1	0	0
1	0	1	0	0
1	1	1	0	0